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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,760	08/30/2001	Philip J. Ireland	M4065.0143/P143-A	7179

24998 7590 07/18/2005

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EXAMINER	
BARRECA, NICOLE M	

ART UNIT	PAPER NUMBER
1756	

DATE MAILED: 07/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,760	IRELAND ET AL.	
	Examiner	Art Unit	
	Nicole M. Barreca	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 23 May 2005.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 32,36,38-40,44-48,50,51,60,61 and 63 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 60 is/are allowed.

6)☒ Claim(s) 32,36,38-40,44-48,50,51,61,63 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 32, 36, 38-40, 42, 44-48, 50, 51, 60, 61 and 63 are pending in this application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 36 and 63 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4. There is no disclosure in the original specification or claims which supports the limitation of an integrated circuit comprising an additional (third) anti-reflective layer formed between the second anti-reflective layer and the dielectric layer, as recited in claim 36.

5. There is no disclosure in the original specification or claims which supports the limitation of an integrated circuit comprising the combination of a first dielectric layer, a first anti-reflective layer, a second dielectric layer formed over the first anti-reflective layer and a second anti-reflective coating layer formed over the second dielectric layer, as recited in claim 63.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 63 is rejected under 35 U.S.C. 102(e) as being anticipated by Sandhu (US 6,713,234)

The applied reference has a common inventor and assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

8. A semiconductor device is fabricated. The device includes reflective layers such as gate electrode 36 and interconnection layer 50. Silicon oxide film 58 is formed over the entire surface and corresponds to the first dielectric. First ARC 60 is formed, followed by BPSG layer 62 (second dielectric). Second ARC 64 is then formed. See col.3, 34-col.4, 17 and Fig. 2-5.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 32, 36-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blatchford (US6200734) in view of Tanaka (US 5,733,712).

11. Blatchford discloses a method for fabricating semiconductor devices in integrated circuits using photolithography. The semiconductor device comprises substrate 10, field oxides 11 (dielectric) of varying topography, metal layer 18 (reflective), antireflection coating 17 and photoresist layer 16. The layer of metal will ultimately be patterned to gate electrodes when the MOSFET device is formed. The antireflection coating 17 comprises three layers 13, 14, 15 of silicon containing oxides such as silicon oxynitrides, each with different indices of refraction (n) and extinction coefficients or absorptions (k). The antireflection layers are used to eliminate the interference patterns caused by the rays reflected by the underlying topography when the photoresist is exposed (col.1, 18-col.2, 64). Antireflective coating 17 comprising 3 layers with different indices of refraction n and extinction coefficients k are used to eliminate the problem of undesirable interference patterns (col.2, 8-32). When there are three antireflection layers, the first antireflection layer 13 is formed with a thickness of 350-450 angstroms (35-45 nm), while the second antireflection layer 15 is formed with a thickness between

150-250 angstroms (15-25 nm). For the first antireflection layer, k1 is between about 1.1-1.9 and for the second antireflection layer, k2 is between about 0.15-0.3. The index of refraction n2 is in the range of 1.7-2.0 (col.4, 49-61). In order to prevent crosslinking between the photoresist layer 16 and the antireflection coating 17, an additional oxynitride layer 19 (dielectric layer) is formed there between (col.3, 8-15).

Blatchford teaches that in general antireflection layers are used to eliminate the interference patterns caused by the rays reflected by the underlying topography when the photoresist is exposed and specifically that antireflective coating 17 comprises 3 layers with different indices of refraction n and extinction coefficients k in order to eliminate the problem of undesirable interference patterns. The reference however does not explicitly state that the amplitudes of the interfaces are approximately equal and that the phase differences of the reflected radiation from the interfaces mutually cancel when combined or that the phase differences are approximately 180 degrees out of phase. Tanaka teaches that the known antireflection method utilizes light interference to prevent reflection and that it is known that the antireflection method using light interference requires that the reflectivity of the interfaces be equal and of the opposite phase in order to cancel the reflected light from these interfaces (col.1, 37-38, col.2, 1-9). Therefore one of ordinary skill in the art would have to expect that the amplitudes of the interfaces are approximately equal and that the phase differences of the reflected radiation from the interfaces mutually cancel when combined or that the phase differences are approximately 180 degrees out of phase in the method of Blatchford which uses three antireflective layers with different indices of refraction n and

extinction coefficients k in order to eliminate the problem of undesirable interference patterns because Tanaka teaches that it is known that the antireflection method using light interference requires that the reflectivity of the interfaces be equal and of the opposite phase in order to cancel the reflected light from these interfaces.

Blatchford teaches that k1 is between about 1.1-1.9, k2 is between about 0.15-0.3 and n2 is in the range of 1.7-2.0 (col.4, 49-61). Blatchford also teaches that the indices of refraction for the antireflective layers are different, but is silent on the specific index of refraction for the first antireflective layer, n1, (for the embodiment where there are three antireflective layers), and does not disclose that the first index of refraction is approximately 2.1. However Blatchford teaches that the indices of refraction are varied in the three layers by varying the ratio of silane to nitrous oxide during the deposition and are designed to with used with a photoresist layer which is exposed to DUV light in order to avoid destructive interference of the reflected rays, thereby establishing the indices of refraction as result-effective variables. It would have been within the ordinary skill of one in the art to determine the optimal index of refraction for the first antireflection layer in Blatchford by routine experimentation and to have the thickness be approximately 2.1, if required, because Blatchford establishes that the index of refraction is a result-effect variable and the discovery of an optimum value of a result effective variable is ordinary within the skill of the art (*In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980)).

12. Claims 40, 42, 44, 45, 47, 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blatchford in view of Fukuda (US 6255151).

13. Blatchford discloses a method for fabricating semiconductor devices in integrated circuits using photolithography. The semiconductor device comprises substrate 10, field oxides 11 (dielectric) of varying topography, metal layer 18 (reflective), antireflection coating 17 and photoresist layer 16. The layer of metal will ultimately be patterned to gate electrodes when the MOSFET device is formed. The antireflection coating 17 comprises three layers 13, 14, 15 of silicon containing oxides such as silicon oxynitrides, each with different indices of refraction (n) and extinction coefficients or absorptions (k). The antireflection layers are used to eliminate the interference patterns caused by the rays reflected by the underlying topography when the photoresist is exposed (col.1, 18-col.2, 64). Antireflective coating 17 comprising 3 layers with different indices of refraction n and extinction coefficients k are used to eliminate the problem of undesirable interference patterns (col.2, 8-32). When there are three antireflection layers, the first antireflection layer 13 is formed with a thickness of 350-450 angstroms (35-45 nm), while the second antireflection layer 15 is formed with a thickness between 150-250 angstroms (15-25 nm). For the first antireflection layer, k1 is between about 1.1-1.9 and for the second antireflection layer, k2 is between about 0.15-0.3. The index of refraction n2 is in the range of 1.7-2.0 (col.4, 49-61). In order to prevent crosslinking between the photoresist layer 16 and the antireflection coating 17, an additional oxynitride layer 19 (dielectric layer) is formed there between (col.3, 8-15). Layer 13 corresponds to the first anti-reflective layer and layer 15 corresponds to the second anti-reflective layer. Layer 17 is formed of silicon oxynitride which is insulating and therefore corresponds to an insulating layer formed on the second anti-reflective layer.

Blatchford is silent on the specific semiconductor device being formed and does not disclose that the semiconductor device comprises a memory cell comprising at least two active areas, a gate stack between the active areas, and a capacitor in electrical contact with one of the active areas (cl.40), or that the structure is a DRAM cell comprising first, second and third active areas, first and second gate stacks and first and second capacitors, the first gate stack being formed between the first and second active areas, the second gate stack being formed between the second and third active areas, the first capacitor being in electrical contact with the first active area, the second capacitor being in electrical contact with the third active area, and the second active area being in electrical contact with a bit line (cl.44), or that the capacitors are formed over the gate stacks (cl.45), or that the bit line is formed over the capacitors (cl.47).

Fukuda teaches that memory cells of a DRAM are generally placed at points where a plurality of word and bit lines intersect on a principal surface of the semiconductor substrate in matrix form. Each memory cell comprises one memory cell section (MISFET) and one capacitor electrically connected in series therewith. The memory cell selection is formed within an active region, is surrounded by a device separation region and comprises a gate oxide, a gate electrode constructed with each word line, and a source/drain pair. Each bit line is placed at an upper portion of the memory cell and is electrically connected to one of the source and drain shared by two adjacent memory cells, while the capacitor is also placed in the upper portion and electrically connected to the other of the source and drain (col.1, 14-33). It would have been obvious to one of ordinary skill in the art to have the semiconductor structure in

Blatchford to additionally include components such as active regions, gate stacks, capacitors and bit lines, arranged as claimed, because Fukada teaches that such components in this arrangement are conventional for a memory cell in the art. While Fukuda does not explicitly disclose that there are three active regions that are specifically arranged as claimed in cl.44, the reference does teach that there are a plurality of memory cells and bit and word lines, arranged in series. It would have been within the- ordinary skill of one in the art to determine the exact number of active regions and cells required for the specific device being manufactured because Fukuda teaches that such memory cells and their general structure are known in the art.

14. Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blatchford in view of Fukuda as applied to claim 45 above, and further in view of Chen (US 6140179).

15. While Blatchford in view of Fukuda teaches capacitors arranged in the memory cell, the references do not disclose that the capacitors are container capacitors. Chen teaches that crown (or container) capacitors conventional in the art (col.2, 23-27, col.3, 5-6). It would have been obvious to one of ordinary skill in the art to have the capacitor in Blatchford in view of Fukuda be a container capacitor because Chen teaches crown (container) capacitors are conventional in the art.

16. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blatchford in view of Lyons (US 6287959) and Fukuda.

17. The teachings of Blatchford have been previously discussed. Blatchford discloses a method for fabricating semiconductor devices in integrated circuits using

photolithography. The semiconductor device comprises substrate 10, field oxides 11 (dielectric) of varying topography, metal layer 18 (reflective), antireflection coating 17 and photoresist layer 16. The antireflection coating 17 comprises three layers 13, 14, 15 of silicon containing oxides such as silicon oxynitrides, each with different indices of refraction (n) and extinction coefficients or absorptions (k). Layer 13 corresponds to the first anti-reflective layer and layer 15 corresponds to the second anti-reflective layer. Layer 17 is formed of silicon oxynitride which is insulating and therefore corresponds to an insulating layer formed on the second anti-reflective layer. Blatchford does not disclose that the silicon oxynitride antireflective layers are an etch stop layer. Lyons teaches that silicon oxynitride can be used as both a successful antireflective layer and etch stop (col.2, 34-41, col.4, 42-49). One of ordinary skill in the art would have to expect that the antireflective layers of silicon oxynitride in Blatchford would additionally function as an etch stop layer because Lyons teaches that that silicon oxynitride can be used as both a successful antireflective layer and etch stop.

Blatchford is silent on the specific semiconductor device being formed and does not disclose that the semiconductor device comprises a memory cell comprising at least two active areas, a gate stack between the active areas, and a capacitor in electrical contact with one of the active areas. Fukuda teaches that memory cells of a DRAM are generally placed at points where a plurality of word and bit lines intersect on a principal surface of the semiconductor substrate in matrix form. Each memory cell comprises one memory cell section (MISFET) and one capacitor electrically connected in series therewith. The memory cell selection is formed within an active region, is surrounded

by a device separation region and comprises a gate oxide, a gate electrode constructed with each word line, and a source/drain pair. Each bit line is placed at an upper portion of the memory cell and is electrically connected to one of the source and drain shared by two adjacent memory cells, while the capacitor is also placed in the upper portion and electrically connected to the other of the source and drain (col.1, 14-33). It would have been obvious to one of ordinary skill in the art to have the structure comprising the semiconductor substrate, antireflection layers, dielectric layer and photoresist layer in Blatchford in view of Lyons to additionally include components such as active regions, gate stacks, capacitors and bit lines, arranged as claimed in claim 50 because Fukada teaches that such components in this arrangement are conventional for a memory cell in the art.

18. Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blatchford in view of Tanaka, Fukada and Podlesny (US 5724299).

19. Blatchford discloses a method for fabricating semiconductor devices in integrated circuits using photolithography. The semiconductor device comprises substrate 10, field oxides 11 (dielectric) of varying topography, metal layer 18 (reflective), antireflection coating 17 and photoresist layer 16. The layer of metal will ultimately be patterned to gate electrodes when the MOSFET device is formed. The antireflection coating 17 comprises three dielectric layers 13, 14, 15 of silicon containing oxides such as silicon oxynitrides, each with different indices of refraction (n) and extinction coefficients or absorptions (k). The antireflection layers are used to eliminate the interference patterns caused by the rays reflected by the underlying topography when the photoresist is

exposed (col.1, 18-col.2, 64). Antireflective coating 17 comprising 3 layers with different indices of refraction n and extinction coefficients k are used to eliminate the problem of undesirable interference patterns (col.2, 8-32). When there are three antireflection layers, the first antireflection layer 13 is formed with a thickness of 350-450 angstroms (35-45 nm), while the second antireflection layer 15 is formed with a thickness between 150-250 angstroms (15-25 nm). For the first antireflection layer, k1 is between about 1.1-1.9 and for the second antireflection layer, k2 is between about 0.15-0.3. The index of refraction n2 is in the range of 1.7-2.0 (col.4, 49-61). In order to prevent crosslinking between the photoresist layer 16 and the antireflection coating 17, an additional oxynitride layer 19 (dielectric layer) is formed there between (col.3, 8-15).

Blatchford teaches that in general antireflection layers are used to eliminate the interference patterns caused by the rays reflected by the underlying topography when the photoresist is exposed and specifically that antireflective coating 17 comprises 3 layers with different indices of refraction n and extinction coefficients k in order to eliminate the problem of undesirable interference patterns. The reference however does not explicitly state that the amplitudes of the interfaces are approximately equal and that the phase differences of the reflected radiation from the interfaces mutually cancel when combined or that the phase differences are approximately 180 degrees out of phase. Tanaka teaches that the known antireflection method utilizes light interference to prevent reflection and that it is known that the antireflection method using light interference requires that the reflectivity of the interfaces be equal and of the opposite phase in order to cancel the reflected light from these interfaces (col.1, 37-38,

col.2, 1-9). Therefore one of ordinary skill in the art would have to expect that the amplitudes of the interfaces are approximately equal and that the phase differences of the reflected radiation from the interfaces mutually cancel when combined or that the phase differences are approximately 180 degrees out of phase in the method of Blatchford which uses three antireflective layers with different indices of refraction n and extinction coefficients k in order to eliminate the problem of undesirable interference patterns because Tanaka teaches that it is known that the antireflection method using light interference requires that the reflectivity of the interfaces be equal and of the opposite phase in order to cancel the reflected light from these interfaces.

Blatchford is silent on the specific semiconductor device being formed and does not disclose that the semiconductor device comprises a memory cell comprising at least two active areas, a gate stack between the active areas, and a capacitor in electrical contact with one of the active areas. Fukuda teaches that memory cells of a DRAM are generally placed at points where a plurality of word and bit lines intersect on a principal surface of the semiconductor substrate in matrix form. Each memory cell comprises one memory cell section (MISFET) and one capacitor electrically connected in series therewith. The memory cell selection is formed within an active region, is surrounded by a device separation region and comprises a gate oxide, a gate electrode constructed with each word line, and a source/drain pair. It would have been obvious to one of ordinary skill in the art to have the semiconductor structure in Blatchford to additionally include components such as active regions, gate stacks, capacitors and bit lines,

arranged as claimed because Fukada teaches that such components in this arrangement are conventional for a memory cell in the art.

The teachings of the references have been discussed above. Blatchford teaches a structure comprising three antireflection layers having different indices of refraction, a dielectric layer and a photoresist layer for use in the manufacture of a semiconductor device, while Fukuda teaches the components and arrangement of a conventional memory cell. The references however do not disclose a computer system comprising a processor and a memory comprising at one memory cell comprising the components as claimed. Podlesny teaches that a memory cell array is typically used as memory for a computer system having a processor (col.6, 42-46). It would have been obvious to one of ordinary skill in the art to have the memory cell including the multiple antireflective layers in Blatchford in view of Tanaka and Fukuda as the memory, along with a processor, in order to form a computer system because Podlesny teaches that it is known in the art to use a memory cell array as memory for a computer system having a processor.

20. Claim 61 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blatchford in view of Lyons.

21. Blatchford discloses a method for fabricating semiconductor devices in integrated circuits using photolithography. The semiconductor device comprises substrate 10, field oxides 11 (dielectric) of varying topography, metal layer 18 (reflective), antireflection coating 17 and photoresist layer 16. The layer of metal will ultimately be patterned to gate electrodes when the MOSFET device is formed. The antireflection coating 17

comprises three dielectric layers 13, 14, 15 of silicon containing oxides such as silicon oxynitrides, each with different indices of refraction (n) and extinction coefficients or absorptions (k). Layers 13, 14, 15 and 19 are all formed of silicon oxynitride, a dielectric material. Layer 13 corresponds to the dielectric layer over the reflective surface, layer 15 corresponds to the first anti-reflective layer, layer 17 corresponds to the second anti-reflective layer. Blatchford does not disclose that the silicon oxynitride antireflective layers are an etch stop layer. Lyons teaches that silicon oxynitride can be used as both a successful antireflective layer and etch stop (col.2, 34-41, col.4, 42-49). One of ordinary skill in the art would have to expect that the antireflective layers of silicon oxynitride in Blatchford would additionally function as an etch stop layer because Lyons teaches that that silicon oxynitride can be used as both a successful antireflective layer and etch stop.

Allowable Subject Matter

22. Claim 60 is allowed.

23. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to teach or suggest an integrated circuit comprising a first silicon dioxide formed over a reflective surface, a first antireflective layer formed over and in contact with the first silicon dioxide, a second antireflective layer formed over and in contact with the first antireflective layer and a second dioxide layer formed over the second antireflective layer.

Response to Arguments

24. The previous rejections have been modified in order to address all new limitations as amended by the applicant. Therefore applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection. However since the pending rejections are similar, any relevant arguments will be addressed below.

25. The applicant argues that claim 51 has been amended to recite allowable subject matter similar to claim 60. However claim 51 recites dielectric layers, not silicon dioxide layers.

26. With respect to claims 32, 36 and 38-39 the applicant argues that Blatchford does not disclose or suggest a dielectric formed on the second anti-reflective layer. Layer 15 is formed of silicon oxynitride and may be considered the dielectric layer formed on the second antireflective layer. Blatchford also teaches forming between the photoresist layer 16 and the antireflection coating 17 (layer 13-15), an additional oxynitride layer 19 or dielectric layer (col.3, 8-15). Therefore layer 19 may be considered the dielectric layer for the embodiment where three antireflective layers are recited in claim 36.

27. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in

the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it is found in the references themselves, as stated in the pending rejections.

28. In response to applicant's argument that Blatchford, Tanka and Fukuda are nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, the prior art is all in the same field of endeavor, the fabrication of semiconductor devices.

29. Please note that Blatchford discloses forming antireflective layers 13, 14 and 15 and forming silicon oxynitride layer 19 over the antireflective layers. All antireflective layers are formed of silicon oxynitride. Therefore any and all of layer 13,14 15 and 19 would be considered dielectric layers. Also please note that the applicant's claims are written in open language and therefore do not limit the presence of additional layers. In addition, claims reciting a layer "over" another layer do not require such layers to be directly in contact.

Conclusion

30. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nicole M. Barreca whose telephone number is 571-272-1379. The examiner can normally be reached on Monday-Thursday (9AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark F. Huff can be reached on 571-272-1385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nicole M Barreca

NICOLE BARRECA
PRIMARY EXAMINER
Art Unit 1756

7/13/05